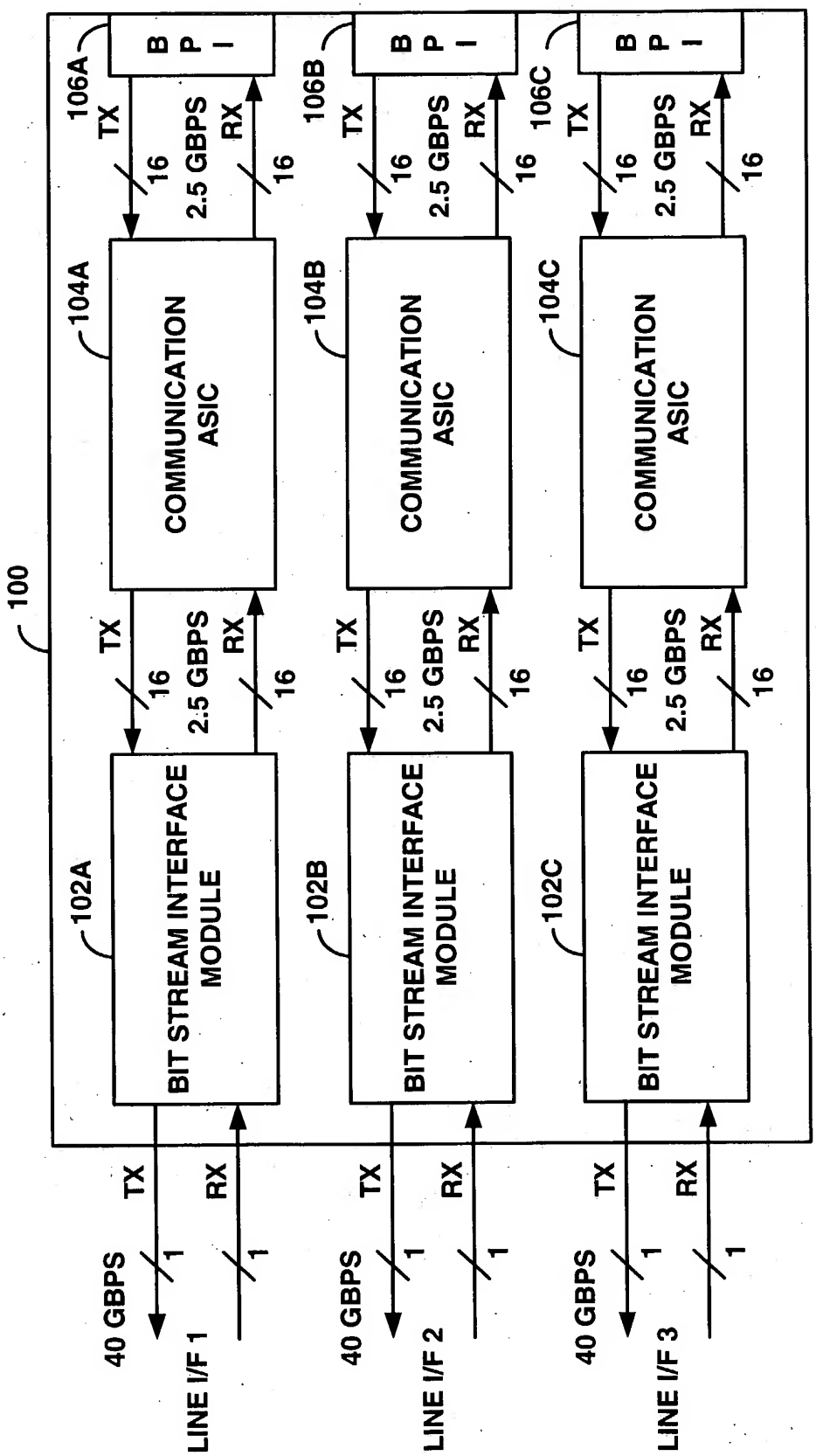

100
102A
BIT STREAM INTERFACE MODULE
102B
BIT STREAM INTERFACE MODULE
102C
BIT STREAM INTERFACE MODULE
104A
COMMUNICATION ASIC
104B
COMMUNICATION ASIC
104C
COMMUNICATION ASIC
106A
106B
106C
B P I
TX
RX
16
2.5 GBPS
40 GBPS
1
LINE I/F 1
LINE I/F 2
LINE I/F 3

FIG. 1

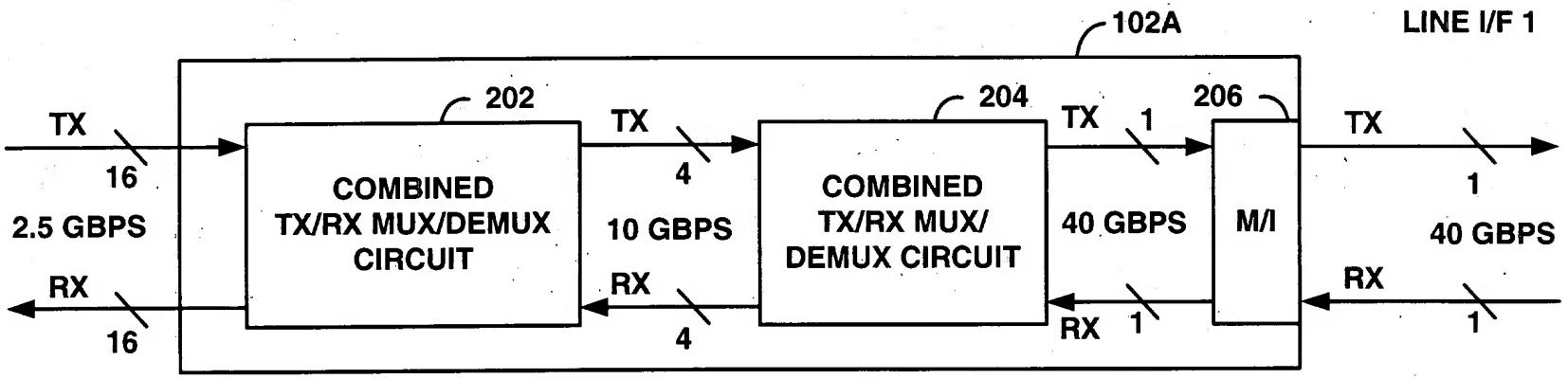

102A
LINE I/F 1
202
204
206
TX
16
2.5 GBPS
RX
16
COMBINED
TX/RX MUX/DEMUX
CIRCUIT
TX
4
10 GBPS
RX
4
COMBINED
TX/RX MUX/
DEMUX CIRCUIT
TX
1
40 GBPS
RX
1
M/I
TX
1
40 GBPS
RX
1

FIG. 2A

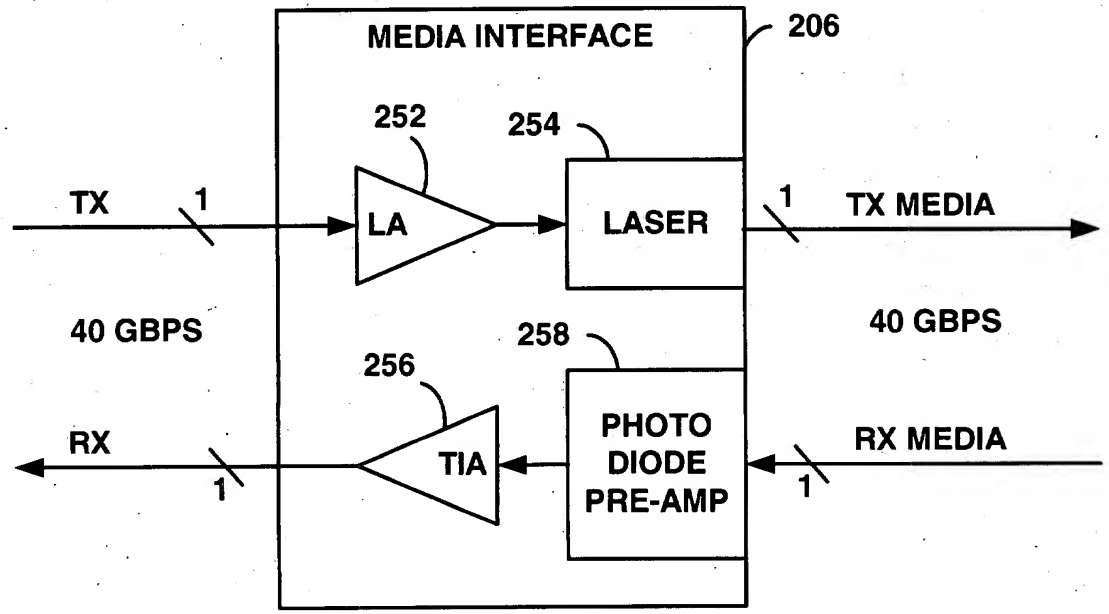

MEDIA INTERFACE
206
252
254
TX
1
40 GBPS
LA
LASER
1
TX MEDIA
40 GBPS
258
256
RX
1
TIA
PHOTO
DIODE
PRE-AMP
RX MEDIA
1

FIG. 2B

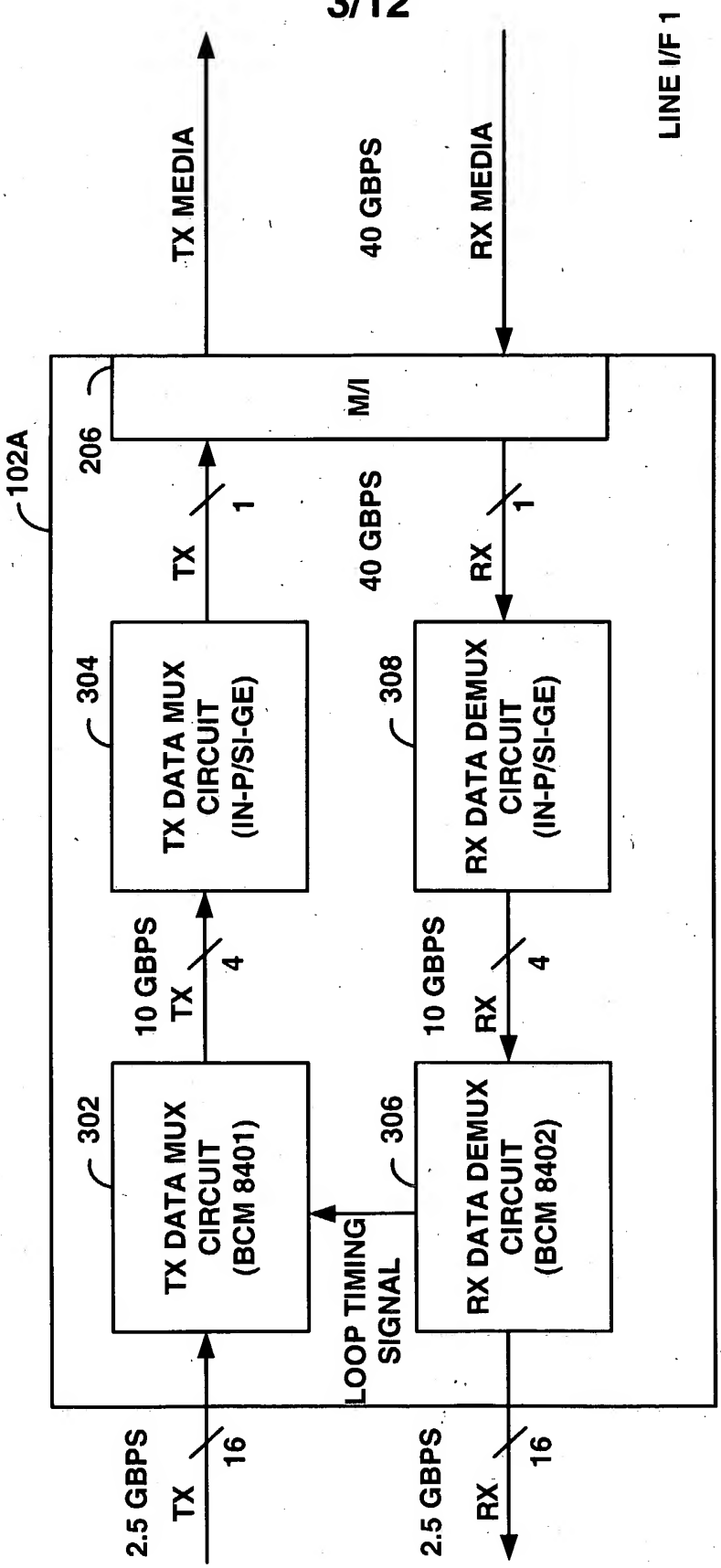

LINE I/F 1
TX MEDIA
40 GBPS
RX MEDIA
102A
206
M/I
TX
1
40 GBPS
RX
1
304
TX DATA MUX CIRCUIT (IN-P/SI-GE)
308
RX DATA DEMUX CIRCUIT (IN-P/SI-GE)
10 GBPS
TX
4
10 GBPS
RX
4
302
TX DATA MUX CIRCUIT (BCM 8401)
306
RX DATA DEMUX CIRCUIT (BCM 8402)
LOOP TIMING SIGNAL
2.5 GBPS
TX
16
2.5 GBPS
RX
16

FIG. 3

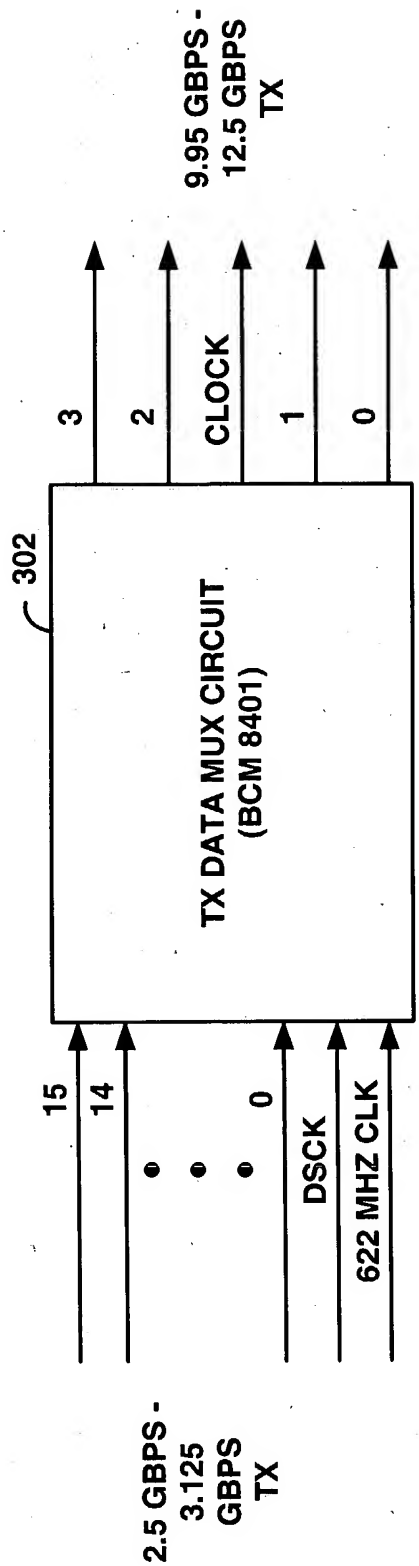

9.95 GBPS - 12.5 GBPS TX
3
2
CLOCK
1
0
302
TX DATA MUX CIRCUIT (BCM 8401)
15
14
0
DSCK
622 MHZ CLK
2.5 GBPS - 3.125 GBPS TX

FIG. 4A

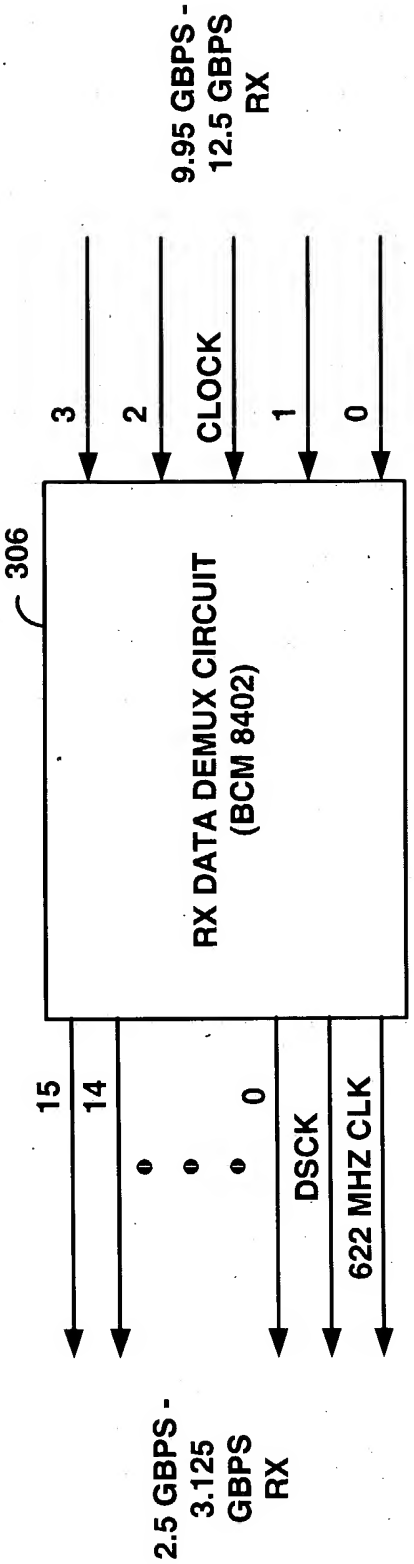

9.95 GBPS - 12.5 GBPS RX
3
2
CLOCK
1
0
306
RX DATA DEMUX CIRCUIT (BCM 8402)
15
14
0
DSCK
622 MHZ CLK
2.5 GBPS - 3.125 GBPS RX

FIG. 4B

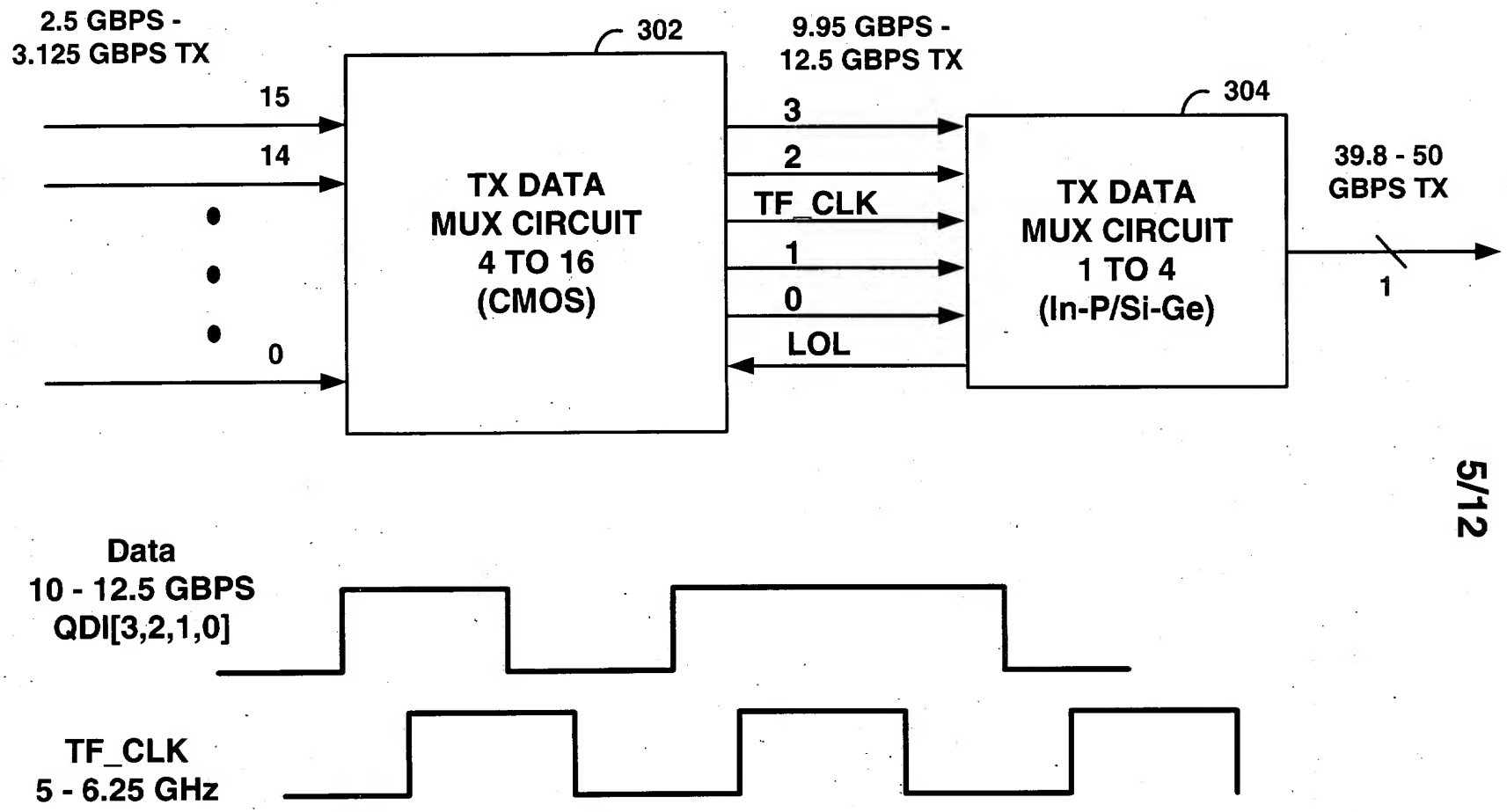

2.5 GBPS -
3.125 GBPS TX
15
14
0
302
TX DATA
MUX CIRCUIT
4 TO 16
(CMOS)
9.95 GBPS -
12.5 GBPS TX
3
2
TF_CLK
1
0
LOL
304
TX DATA
MUX CIRCUIT
1 TO 4
(In-P/Si-Ge)
39.8 - 50
GBPS TX
1
Data
10 - 12.5 GBPS
QDI[3,2,1,0]
TF_CLK
5 - 6.25 GHz

FIG. 5

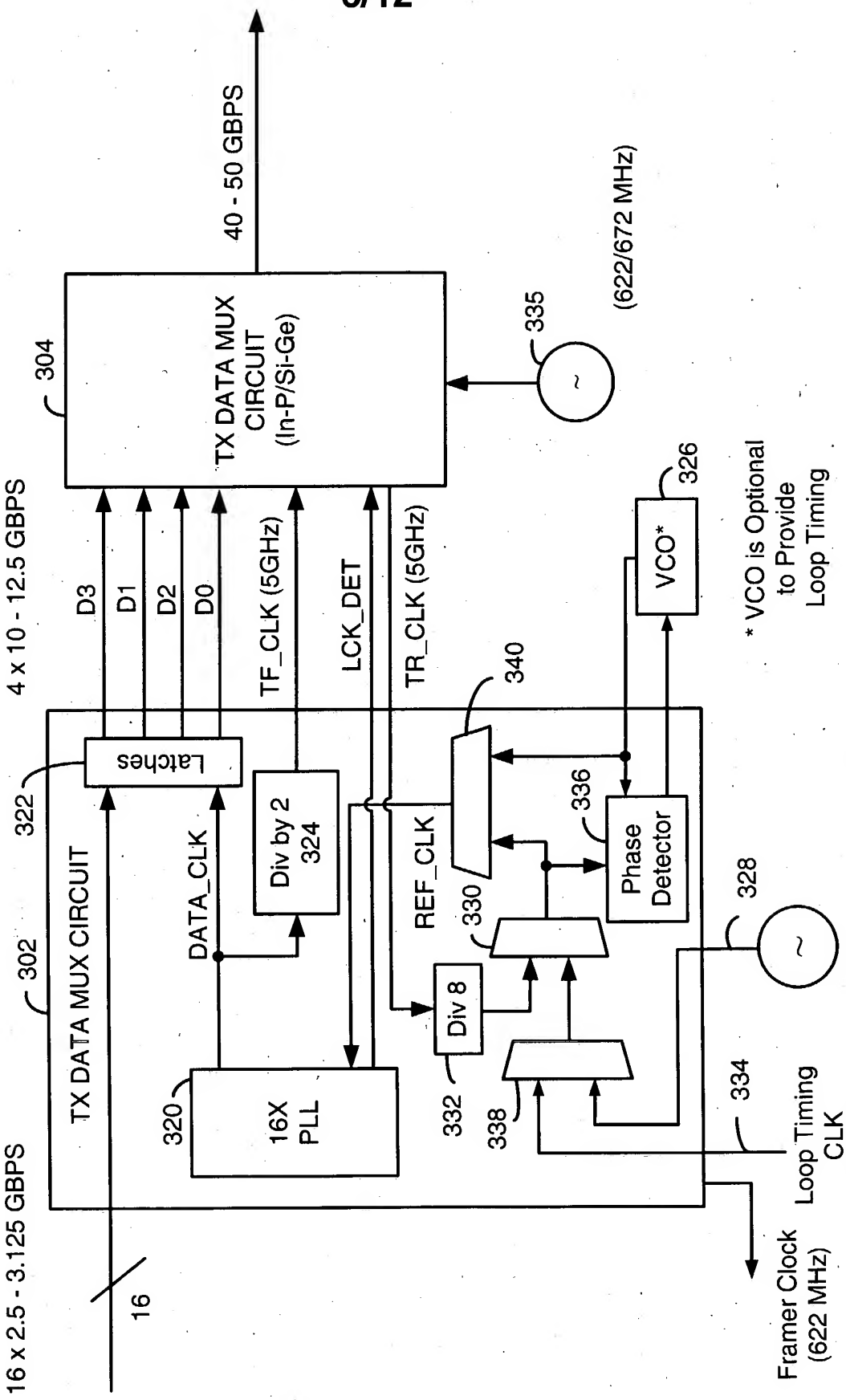

16 x 2.5 - 3.125 GBPS
16
TX DATA MUX CIRCUIT
302
Latches
322
4 x 10 - 12.5 GBPS
D3
D1
D2
D0
DATA_CLK
TF_CLK (5GHz)
LCK_DET
TR_CLK (5GHz)
Div by 2
324
320
16X
PLL
REF_CLK
340
330
Div 8
332
338
336
Phase
Detector
VCO*
326
328
334
Loop Timing
CLK
(622 MHz)
(622/672 MHz)
Framer Clock
(622 MHz)
TX DATA MUX
CIRCUIT
(In-P/Si-Ge)
304
40 - 50 GBPS
335
(622/672 MHz)
* VCO is Optional
to Provide
Loop Timing

FIG. 6A

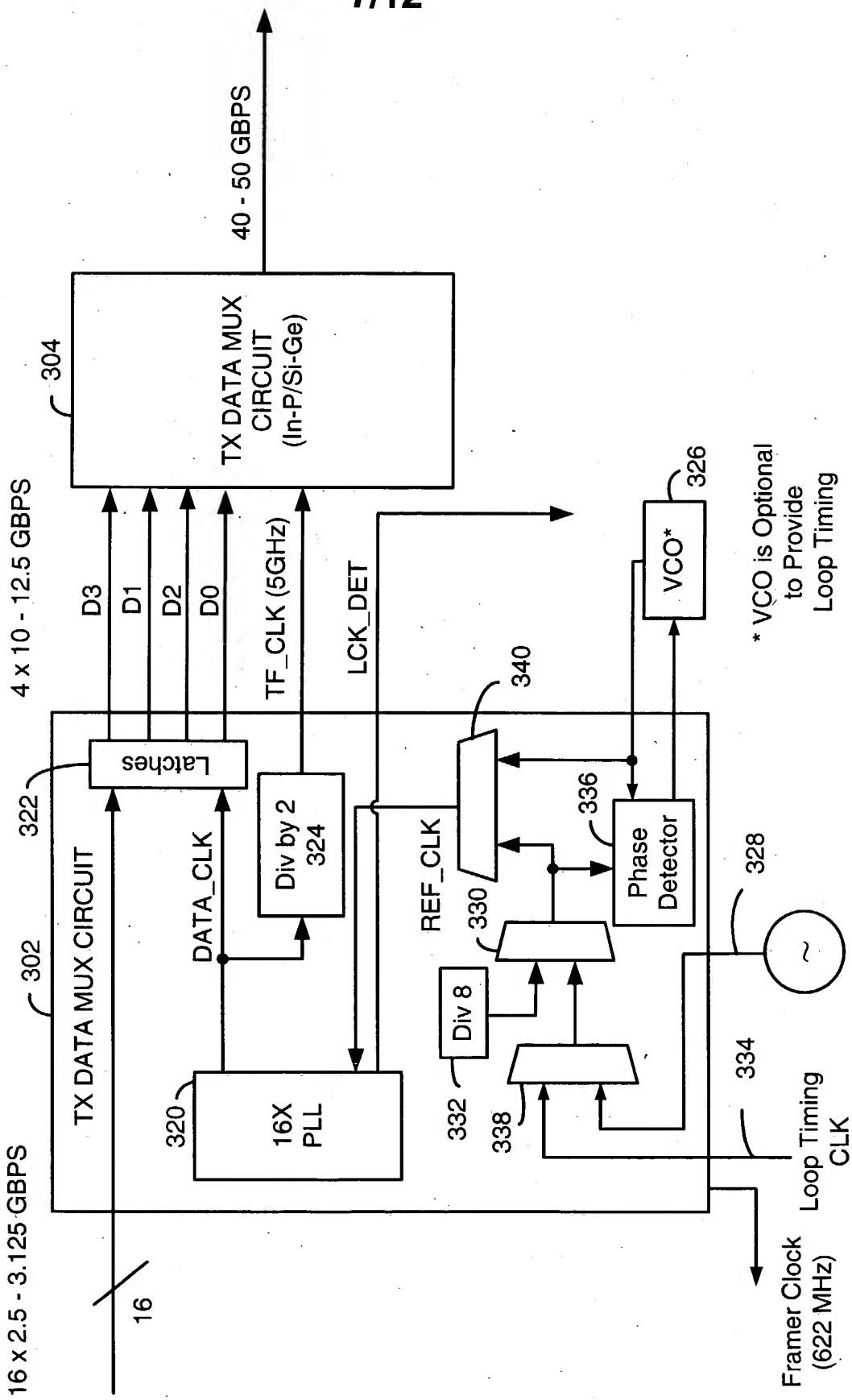

40 - 50 GBPS
304
TX DATA MUX CIRCUIT (In-P/Si-Ge)
4 x 10 - 12.5 GBPS
D3
D1
D2
D0
TF_CLK (5GHz)
LCK_DET
326
VCO*
* VCO is Optional to Provide Loop Timing
340
322
Latches
Div by 2 324
336
Phase Detector
328
REF_CLK
330
DATA_CLK
302
TX DATA MUX CIRCUIT
Div 8
320
16X PLL
332
338
334
16 x 2.5 - 3.125 GBPS
16
Framer Clock (622 MHz)
Loop Timing CLK (622 MHz)
(622/672 MHz)

FIG. 6B

Receiver Input and Source Centered Clock Performance

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Output Common Mode	Vcm	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z_{SE}		40	50	60	Ω
Differential Input impedance	Z_d		80	100	120	Ω
Input Impedance Mismatch	Z_M				10	%
Q40, CML Input Differential Amplitude, p-p	Δ VQDO	See Figure Below	400	500	600	mV
Q40 Input Rise and Fall Time (20% to 80%)	t_{RH} , t_{FH}			25	35	ps
Differential output return loss*	S11	Up to 7.5 GHz	10			dB
4-by-1 mux input return loss >15 db at 10 GHz						

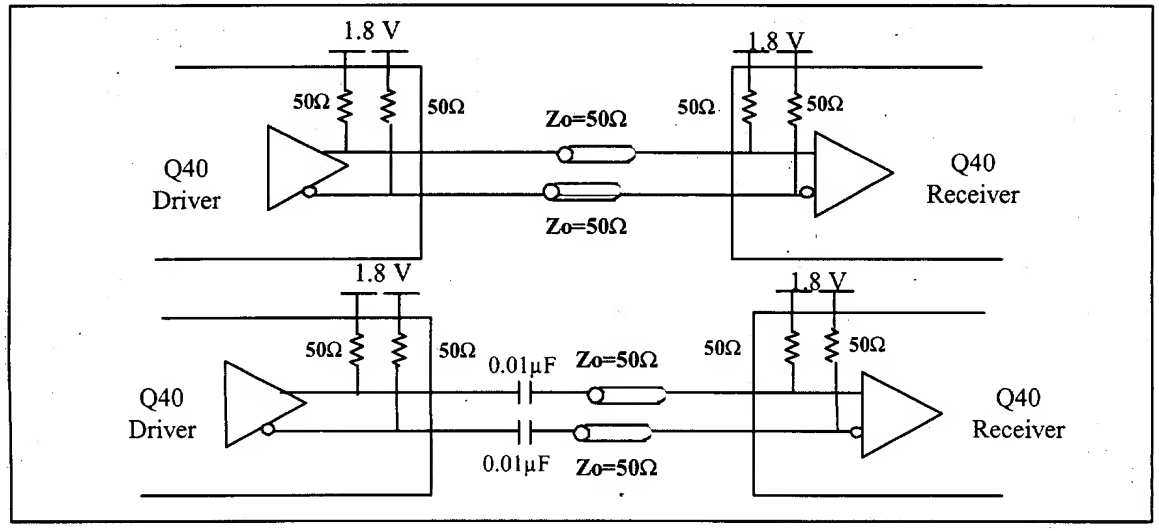
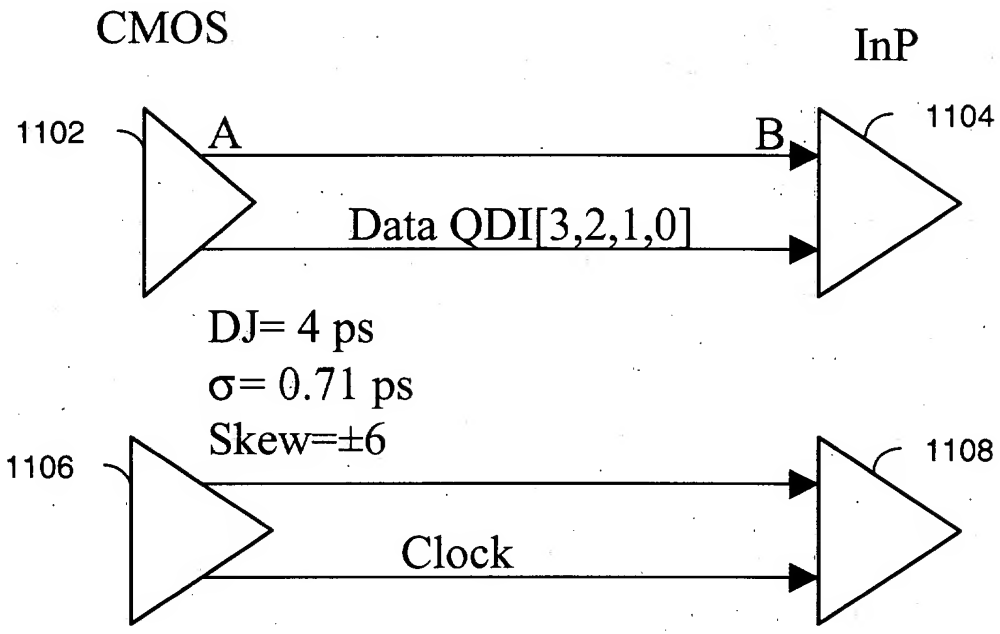


FIG. 7



Additional Sources:
Crosstalk = 4 ps
PCB Mismatch = 4 ps

At B: Total Input Jitter = 4+4+12+4+4+4+0.71*14= 42 ps
CMOS Input Mismatch + setup/Hold = 24 ps
Margin at 10 Gig = 32 ps
Margin at 12.5 Gig = 12 ps

FIG. 8

Transmit and Receive

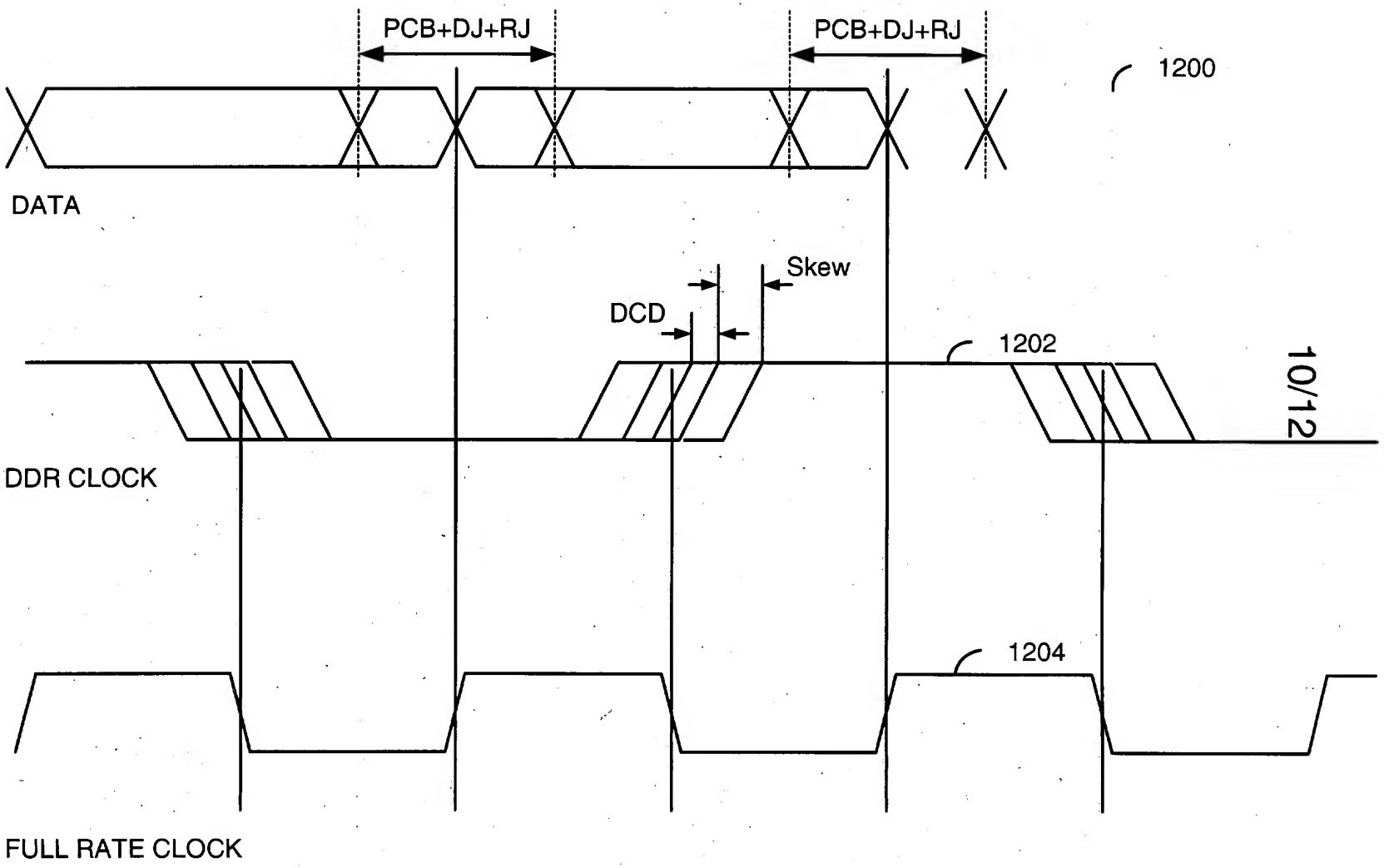


FIG. 9

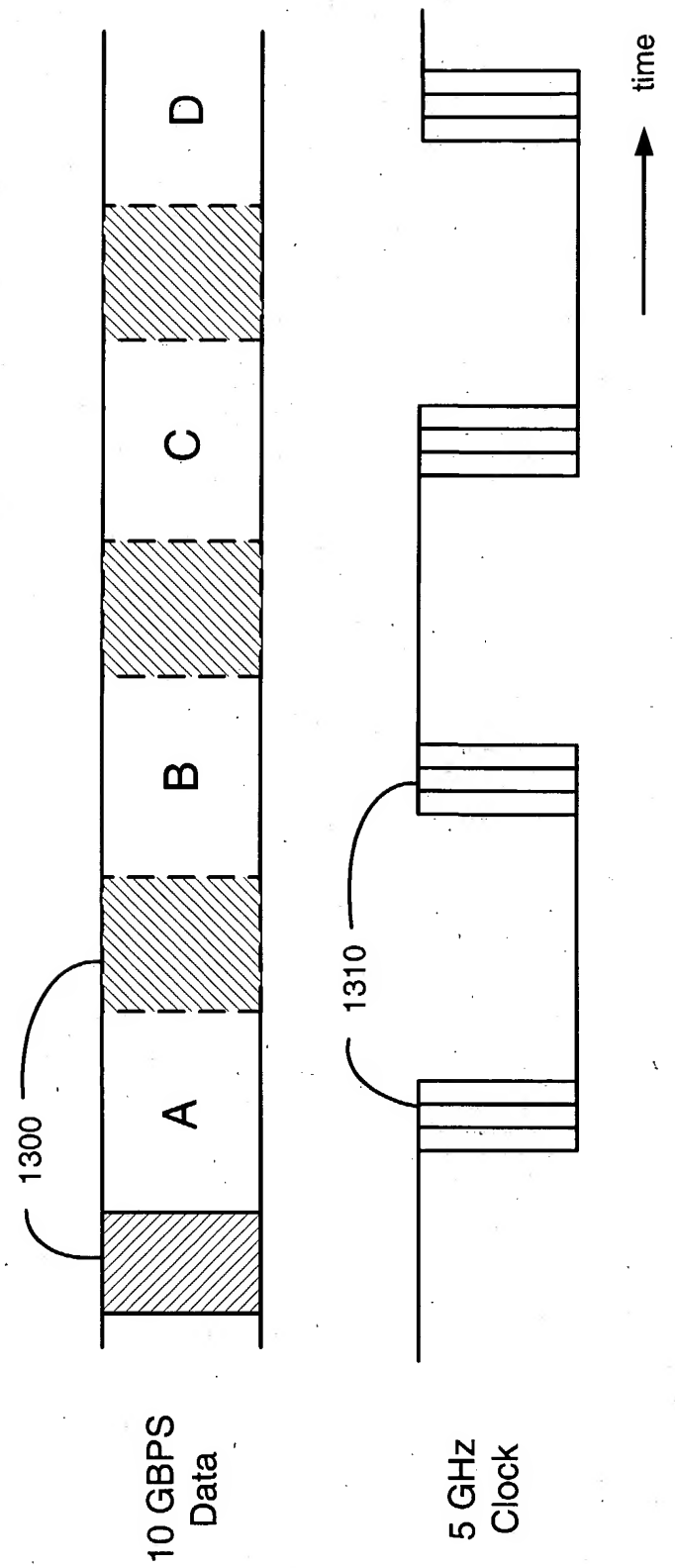


FIG. 10

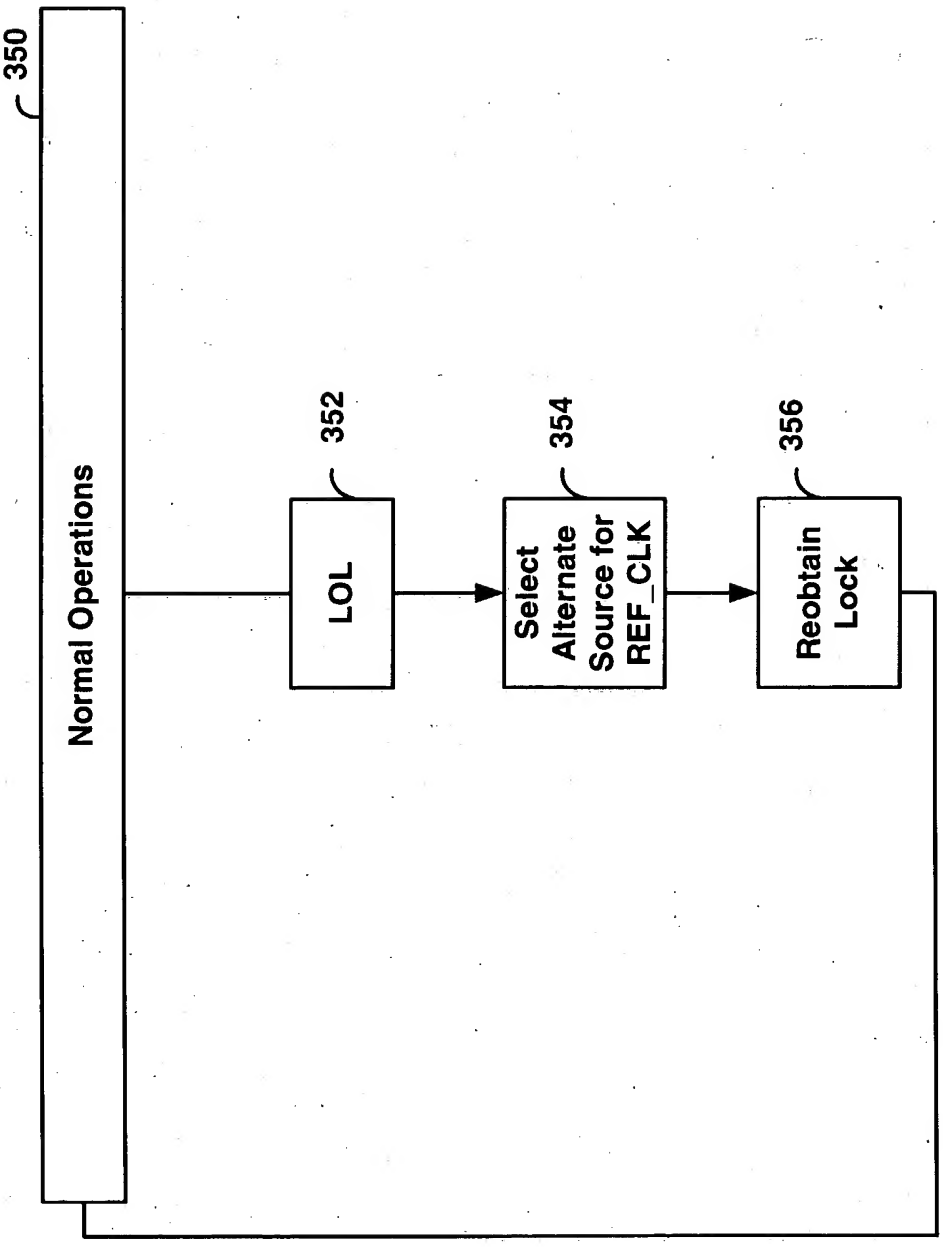

350
Normal Operations
352
LOL
354
Select Alternate Source for REF_CLK
356
Reobtain Lock

FIG. 11